REMARKS

Claims 1, 7, 12 and 18 have been amended to improve form. Claims 1-20 remain pending in this application.

Initially, the applicants note that an Information Disclosure Statement (IDS), PTO-1449 and IDS transmittal letter were filed on January 22, 2004 and a subsequent IDS, PTO-1449 and IDS transmittal letter were filed on August 18, 2004. The Patent Application Retrieval (PAIR) system shows that these documents have been received. The present Office Action, however, has not returned an initialed copy of the PTO-1449s indicating that the listed documents have been officially considered. The applicants also note that another IDS and PTO-1449 were filed on April 15, 2005, subsequent to the issuance of the present Office Action. The applicants respectfully request that the Examiner consider the documents listed on the PTO-1449s filed January 22, 2004, August 18, 2004 and April 15, 2005 and return copies with the next communication with the Examiner's initials indicating that the documents listed on these PTO-1449s have been officially considered.

Claims 1-20 have been rejected under 35 U.S.C. § 102(e) as being unpatentable over Fried et al. (U.S. Patent No. 6,583,469; hereinafter Fried). The rejection is respectfully traversed.

Claim 1 recites a method of manufacturing a semiconductor device that includes forming a fin structure on an insulator. Claim 1, as amended, also recites forming a gate structure over a portion of the fin structure, the gate structure comprising a semiconducting material or a metal. Fried does not disclose or suggest this feature.

For example, the Office Action states that Fried discloses forming a gate structure over a portion of the fin structure and points to Fig. 12B for support (Office Action – page 2). The applicants assume that layers 20, 22 and 24 in Fried are alleged to be equivalent to the claimed gate

structure. Fried discloses that layer 20 is an insulating layer formed over layer 10u (Fried – col. 4, lines 63-66). Fried also discloses that layer 22 is a planarizing layer, such as an anti-reflective coating formed on layer 20 (Fried – col. 5, lines 18-22 and Fig. 7B). Fried further discloses that layer 24 is a photoresist layer formed over layer 22 (Fried – col. 5, lines 31-34 and Fig. 8B). Fried, therefore, does not disclose that any of layers 20, 22 and 24 include a semiconducting material or a metal, as required by amended claim 1.

Claim 1, as amended, also recites removing the semiconducting material or the metal in the gate structure. The Office Action states that Fried disclose removing material 20 and 24 in the gate structure and points to Figs. 12A, 14A and 15 for support (Office Action – page 2). Layers 20 and 24, as discussed above, do not include a semiconducting material or a metal. Therefore, Fried does not disclose removing any semiconducting material or metal in a gate structure, as required by amended claim 1.

Claim 1, as amended, further recites depositing a metal to replace the removed semiconducting material or metal in the gate structure. Since Fried does not disclose the claimed removing, Fried cannot disclose depositing a metal to replace the removed semiconducting material or metal, as required by claim 1.

For at least these reasons, Fried does not disclose or suggest each of the features of amended claim 1. Accordingly, withdrawal of the rejection of claim 1 based on Fried is respectfully requested.

Claims 2-11 depend on claim 1 and are believed to be allowable over Fried for at least the reasons claim 1 is allowable over Fried. In addition, these claims recite additional features not disclosed or suggested by Fried.

For example, claim 4 recites that the method includes after said removing and before said reducing, removing the oxide layers on sides of the silicon fin. The Office Action has not particularly addressed this claim. The applicants respectfully request that any subsequent communication point out where Fried allegedly discloses this feature or withdraw the rejection. In any event, Fried does not disclose or suggest this feature. For at least this additional reason, withdrawal of the rejection and allowance of claim 4 are respectfully requested.

Claim 9 recites that the reducing includes reducing the width of the portion of the fin structure by about 30 nm to about 80 nm in a channel region of the semiconductor device. The Office Action has not particularly addressed this claim. The applicants respectfully request that any subsequent communication point out where Fried allegedly discloses this feature or withdraw the rejection. In any event, Fried may disclose that fin 12 is etched such that the vertical sidewalls of fin 12 are aligned with the vertical sidewalls of oxide layer 16, as illustrated in Fig. 14B (Fried – col. 6, lines 20-26). Fried, however, does not disclose any particular amount by which the width of fin 12 is reduced. Therefore, Fried does not disclose reducing the width of fin 12 by about 30 nm to about 80 nm in a channel region, as required by claim 9. The applicants further assert that Fried cannot be fairly construed to suggest this feature since Fried is totally silent with respect to the amount by which fin 12 is etched.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 9 are respectfully requested.

Claim 12 recites features similar to claim 1. For example, claim 12, as amended, recites forming a gate structure over the fin and the gate oxide, the gate structure comprising a semiconducting material. Claim 12, as amended, also recites removing the semiconducting material

in the gate structure to define a gate recess. Similar to the discussion above with respect to claim 1, Fried does not disclose or suggest these features.

For at least these reasons, withdrawal of the rejection of claim 12 based on Fried is respectfully requested.

Claims 13-17 depend on claim 12 and are believed to be allowable over Fried for at least the reasons claim 12 is allowable over Fried. In addition, these claims recite additional features not disclosed or suggested by Fried.

For example, claim 14 recites features similar to claim 9. For reasons similar to those discussed above with respect to claim 9, withdrawal of the rejection and allowance of claim 14 are respectfully requested.

Claim 15 recites that the forming includes forming the fin with a width between about 40 nm and about 100 nm. The Office Action has not particularly addressed this claim. The applicants respectfully request that any subsequent communication point out where Fried allegedly discloses this feature or withdraw the rejection. In any event, Fried is totally silent with respect to the width of fin 12. Therefore, Fried cannot be construed to disclose or suggest forming a fin to the width recited in claim 15. For at least this additional reason, withdrawal of the rejection and allowance of claim 15 are respectfully requested.

Claim 16 recites that the reducing includes reducing the width of the portion of the fin to a width between about 10 nm and about 50. The Office Action has not particularly addressed this claim. The applicants respectfully request that any subsequent communication point out where Fried allegedly discloses this feature or withdraw the rejection. In any event, as discussed above with respect to claim 15, Fried is totally silent with respect to the width of fin 12. Therefore, Fried cannot be construed to disclose or suggest reducing the width of the portion of the fin to the width

recited in claim 16. For at least this additional reason, withdrawal of the rejection and allowance of claim 16 are respectfully requested.

Claim 18, as amended, recites features similar to claim 1. For example, claim 18 recites forming a gate structure over the fin and dielectric cap, the gate structure comprising a semiconducting material or a metal. Similar to the discussion above with respect to claim 1, Fried does not disclose or suggest this feature.

Claim 18, as amended, also recites removing the gate oxide layers from the opposite sides of the fin to expose the fin from the dielectric cap down to the insulator. The Office Action states that Fried discloses forming gate oxide layers 16 and 30 and removing these layers from the opposite side of fin 12 (Office Action – page 3). Fried may disclose planarizing a portion of layers 16 and 30 located above the surface of gate electrode 32 as illustrated in Fig. 18B. Fried, however, does not disclose or suggest removing gate oxide layers 16 and 30 to expose fin 12, much less expose fin 12 from cap 16 down to layer 10u.

For at least these reasons, withdrawal of the rejection of claim 18 based on Fried is respectfully requested.

Claims 19 and 20 depend on claim 18 and are believed to be allowable over Fried for at least the reasons claim 18 is allowable over Fried. In addition, these claims recite additional features not disclosed or suggested by Fried.

For example, claim 19 recites features similar to claim 9 and claim 20 recites features similar to claims 15 and 16. For reasons similar to those discussed above with respect to claim 9, 15 and 16, withdrawal of the rejection and allowance of claims 19 and 20 are respectfully requested.

Claims 1-20 have also been rejected under 35 U.S.C. § 102(e) as being unpatentable over Yang et al. (U.S. Patent No. 6,787,854; hereinafter Yang). The rejection is respectfully traversed.

Claim 1, as amended and as discussed above, recites a method of manufacturing a semiconductor device that includes forming a gate structure over a portion of the fin structure, the gate structure comprising a semiconducting material or a metal. Claim 1, as amended, also recites removing the semiconducting material or the metal in the gate structure and depositing a metal to replace the removed material in the gate structure.

The Office Action states that Yang discloses removing material 410 in the gate structure and depositing a metal to replace the removed material in the gate structure and points to Figs. 4 and 6-8 and col. 6, lines 20-45 for support (Office Action – pages 2-3). The applicants respectfully disagree.

Yang at Fig. 4 discloses that gate material 410 may be deposited and etched to form a gate (Yang – col. 4, lines 33-43). Yang at Figs. 6-8 discloses a different implementation than that in Fig. 4 in which a FinFET with vertically doped source/drain junctions is formed (Yang – col. 5, lines 8-25). This portion of Yang does not disclose depositing a metal to replace removed semiconducting material or metal in a gate structure, as required by claim 1. Yang at col. 6, lines 20-45 corresponds to claims 1-5 of Yang. None of claims 1-6 of Yang discloses depositing a metal to replace removed semiconducting material or metal in a gate structure, as required by claim 1.

For at least these reasons, Yang does not disclose each of the features of claim 1. Accordingly, withdrawal of the rejection and allowance of claim 1 are respectfully requested.

Claims 12 and 18, as discussed above, recite features similar to claim 1. For reasons similar to those discussed above with respect to claim 1, Yang does not disclose or suggest each of the features of claims 12 and 18. Accordingly, withdrawal of the rejection and allowance of claims 12 and 18 are respectfully requested.

Claims 2-11, 13-17, 19 and 20 variously depend on claims 1, 12 and 18 and are believed to be allowable over Yang for at least the reasons their respective independent claims are allowable. Accordingly, withdrawal of the rejection and allowance of claims 2-11, 13-17, 19 and 20 are respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, the applicants respectfully request withdrawal of the outstanding rejection and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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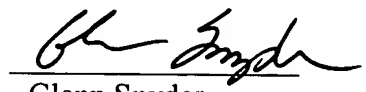
By: 
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